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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/916,924	07/27/2001	Shuaibin Lin	5201-23200	8766

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EXAMINER	
GARCIA OTERO, EDUARDO	
ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 02/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/916,924	LIN, SHUAIBIN	
	Examiner	Art Unit	
	Eduardo Garcia-Otero	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 July 2001 and 09 October 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 October 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION: Non-Final (first action on the merits)

Introduction

1. Title is: SYSTEM AND METHOD FOR STATE RESTORATION IN A DIAGNOSTIC MODULE FOR A HIGH-SPEED MICROPROCESSOR.
2. First listed inventor is: LIN.
3. Claims 1-19 are pending.
4. US Application received 7/27/2001, and no earlier priority is claimed.

Index of Important Prior Art

5. **Fletcher** refers to Engineering Approach to Digital Design by William I. Fletcher, Prentice-Hall, Inc., 1980, pages 276-279.
6. **Tabak** refers to Advanced Microprocessors by Danial Tabak, McGraw-Hill, Second Edition, 1995, ISBN 0-07-062843-2, pages 28, 67, 139, 145, 363, and 466.

Definitions

7. **"Halt"** is defined as "System control instructions permit the user to influence directly the operation of the processor and other subsystems such as the MMU and the cache. Practically all systems have a HLT (halt) instruction that stops the operation of the processor...." and "The halt (HLT) instruction stops the execution of all instructions and places the processor in a halt state. An interrupt or a reset signal will cause the processor to resume execution. The LOCK instruction...". Advanced Microprocessors by Danial Tabak, McGraw-Hill, Second Edition, 1995, ISBN 0-07-062843-2, pages 28, and 139.
8. **"Interrupt"** as "n. A signal from a device to a computer's processor requesting attention from the processor. When the processor receives an interrupt, it suspends its current operations, saves the status of its work, and transfers control to a special routine known as an interrupt handler, which contains the instructions for dealing with the particular situation that caused the interrupt. Interrupts can be generated by various hardware devices to request service or report problems, or by the processor itself in response to program errors or requests for operating system services. Interrupts are the processor's way of communicating with the other elements that make up a computer system. A hierarchy of interrupt priorities determines which interrupt request will be handled first if more than one request is made. A program can temporarily disable some interrupts if it needs the full attention of the processor

to complete a particular task. See also exception, external interrupt, hardware interrupt, internal interrupt, software interrupt." Microsoft Computer Dictionary, Fourth Edition, by Microsoft Press, JoAnne Woodcock as Senior Contributor, ISBN 0-7356-0615-3, May 1999

9. **"Microprocessor"** is defined as "A central processing unit (CPU) on a single chip. A modern microprocessor can have several million transistors in an integrated-circuit package that can easily fit into the palm of one's hand. Microprocessors are at the heart of all personal computers. When memory and power are added to a microprocessor, all the pieces, excluding peripherals, required for a computer are present...". Microsoft Computer Dictionary, Fourth Edition, by Microsoft Press, JoAnne Woodcock as Senior Contributor, ISBN 0-7356-0615-3, May 1999.
10. **"Module"** is defined as "1. In programming, a collection of routines and data structures that performs a particular task or implements a particular abstract data type. Modules usually consist of two parts: an interface, which lists the constants, data types, variables, and routines that can be accessed by other modules or routines, and an implementation, which is private (accessible only to the module) and which contains the source code that actually implements the routines in the module. See also abstract data type, information hiding, Modula-2, modular programming. 2. In hardware, a self-contained component that can provide a complete function to a system and can be interchanged with other modules that can provide similar functions. See also memory card, SIMM." Microsoft Computer Dictionary, Fourth Edition, by Microsoft Press, JoAnne Woodcock as Senior Contributor, ISBN 0-7356-0615-3, May 1999.
11. **"Restore"** is defined as "After a return, and when the register file was out of windows, we have a window underflow. Software must restore previously used register windows in this case. A window overflow trap is caused by the overflow." Advanced Microprocessors by Danial Tabak, McGraw-Hill, Second Edition, 1995, ISBN 0-07-062843-2, pages 363-364.
12. **"Restore[1]"** is defined as "The act of restoring a file or files. See also backup, recovery." Microsoft Computer Dictionary, Fourth Edition, by Microsoft Press, JoAnne Woodcock as Senior Contributor, ISBN 0-7356-0615-3, May 1999.
13. **Restore[2]"** is defined as "To copy files from a backup storage device to their normal location, especially if the files are being copied to replace files that were accidentally lost or deleted."

Microsoft Computer Dictionary, Fourth Edition, by Microsoft Press, JoAnne Woodcock as Senior Contributor, ISBN 0-7356-0615-3, May 1999.

14. **"Software interrupt"** as "n. A program-generated interrupt that stops current processing in order to request a service provided by an interrupt handler (a separate set of instructions designed to perform the task required). Also called trap." Microsoft Computer Dictionary, Fourth Edition, by Microsoft Press, JoAnne Woodcock as Senior Contributor, ISBN 0-7356-0615-3, May 1999

15. **"State Machine"** is defined as "some system that generates control outputs, which are a function of the present input conditions and, just as important, the past history of these inputs" and "SEQUENTIAL MACHINE or a FINITE STATE MACHINE (FSM)". Engineering Approach to Digital Design by William I. Fletcher, Prentice-Hall, Inc., 1980, pages 276, 279.

Duplicate Claim Warning

16. Applicant is advised that should claim 1 be found allowable, claim 15 will be objected to under 37 CFR 1.75 as being a substantial duplicate thereof. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

17. Note the preamble of claim 1 states "A diagnostic system associated with a microprocessor, comprising", and the preamble of claim 15 states "A microprocessor, with an associated diagnostic module, said module comprising". Thus, both preambles appear to claim "machines" per 35 USC 101, and both claims have the same limitations.

18. The same duplicate claim warning applies to the dependent claims of claim 1 and claim 15.

35 USC § 101-statutory subject matter-Data Structures Per Se

19. 35 U.S.C. 101 reads as follows: Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

20. Claim 1, 8, 9, and 15 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

21. In claim 1, the third limitation ("state restoration logic...") appears to be a data structure per se, and is nonstatutory. See MPEP 2106(IV)(B)(1) "claim to a data structure per se held nonstatutory".
22. Note that the claim 1 preamble term "system" is ambiguous with respect to which statutory category of 35 USC 101 (process, machine, manufacture, or composition of matter, or any new and useful improvement) is intended. The ambiguous preamble term "system" often foreshadows 35 USC 101 rejections, and 35 USC 112 rejections, and duplicate claim warnings as in these claims. Additionally, using vague and ambiguous terminology frequently results in a single claim which improperly claims both a machine and a process for using the machine (although that did not occur in these claims), see MPEP 2173.05(p)(II).
23. Thus, the Examiner suggests that it may be preferable to use the 35 U.S.C. § 101 statutory terms ("process", "machine", etc.) or well known equivalent terms ("apparatus" and "method"), and to avoid potentially vague and ambiguous terms such as "system".
24. The claim 1 first limitation ("a state machine") and second limitation ("a backup register") clearly indicate machine elements. Thus, the preamble term "system" is interpreted as a machine per 35 USC 101.
25. However, the third limitation "state restoration logic..." is a data structure per se, and is nonstatutory. Note that MPEP 2106(IV)(B)(1) also states "When functional descriptive material is recorded on some computer-readable medium it becomes structurally and functionally interrelated to the medium ands will be statutory in most cases since use of technology permits the function of the descriptive material to be realized."
26. Thus, the Examiner suggests amending claim 1 to embody the logic on a computer-readable medium.
27. In claim 8, the limitation "a trace function" is rejected for the same reasons as claim 1.
28. Claims 9 and 15 are rejected for the same reasons as claim 1.

35 USC § 112-Second Paragraph-indefinite claims

29. The following is a quotation of the second paragraph of 35 U.S.C. 112: The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

30. Claims 1, 3, and 15 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.
31. In claim 1, the preamble term "A diagnostic system associated with a microprocessor" is not clear. Specifically, it is not clear whether the microprocessor is part of the claimed invention, or whether the term "associated with a microprocessor" is a mere intended use of the "system", or perhaps is a feature of the "system" described by functional limitations. Note MPEP 2114 "features of an apparatus may be recited either structurally or functionally".
32. Further, it is not clear whether the preamble term of claim 1 is intended to be different from the preamble term of claim 15 ("A microprocessor, with an associated diagnostic module"). See the above duplicate claim warnings. Claim 15 is rejected for the same reason.
33. Also in claim 1, the term "trigger event is invalid" is not clear. See definitions of "interrupt" and "software interrupts" above.
34. In claim 2, the term "the trigger events comprise specified memory addresses" is not clear. An "event" means some kind of action or occurrence, whereas "specified memory addresses" is a noun. Possibly an event might be writing to a specific address, or reading from a specific address, but this is far from clear. Even under this possible interpretation, it would is not clear how or when or why specific addresses are specified.
35. In claim 3, the term "trigger events further comprise specified data values" is not clear, for the same reasons as claim 2.
36. In claim 12, the term "the microprocessor is equipped with an instruction pipeline" appears very similar to a machine element limitation, however claim 12 depends from "method" claim 9. It is not clear how this limitation is intended as a method limitation. See MPEP 2173.05(p)(II), see 35 USC 101.

Claim Rejections - 35 USC § 103

37. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action: (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

38. The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows: Determining the scope and contents of the prior art. Ascertaining the differences between the prior art and the claims at issue. Resolving the level of ordinary skill in the pertinent art. Considering objective evidence present in the application indicating obviousness or nonobviousness.
39. Claim 1-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fletcher in view of Tabak.
40. Independent claim 1 is a "diagnostic system" claim with 3 limitations, numbered by the Examiner for clarity.
41. In claim 1 limitation 1, "a state machine" is disclosed by Fletcher page 279 "FINITE STATE MACHINE". Note Fletcher page 276 states "By using these feedback, ideally the output of a controlled system at some time t_0 is the resultant of both the input conditions at t_0, combined with all the input conditions leading up to t_0".
42. Fletcher does not expressly disclose the additional limitations.
43. In claim 1 limitation 2, "restore" is disclosed by Taback page 363 "After a return, and when the register file was out of windows, we have a window underflow. Software must restore previously used register windows in this case. A window overflow trap is caused by the overflow."
44. In claim 1 limitation 3, "state restoration logic" is disclosed by Taback page 363 "After a return, and when the register file was out of windows, we have a window underflow. Software must restore previously used register windows in this case. A window overflow trap is caused by the overflow."
45. At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to use Tabak to modify Fletcher. One of ordinary skill in the art would have been motivated to do this in order to replace files that were accidentally lost or deleted.
46. Claims 2-8 depend from claim 1.
47. In claim 2, "trigger events comprise specified memory addresses" is disclosed by Taback page 363 "After a return, and when the register file was out of windows, we have a window underflow. Software must restore previously used register windows in this case. A window overflow trap is caused by the overflow."

48. In claim 3, "trigger events further comprise specified data values" is disclosed by Taback page 363 "After a return, and when the register file was out of windows, we have a window underflow. Software must restore previously used register windows in this case. A window overflow trap is caused by the overflow."
49. In claim 4, "the microprocessor is equipped with an instruction pipeline" is disclosed by Tapak page 67 "pipeline".
50. In claim 5, "exception handler" is disclosed by Taback page 145 "interrupt".
51. In claim 6, "the trigger event is invalid whenever the branch instruction is re-executed upon returning from the exception handler" is disclosed by Taback page 145 "interrupt".
52. In claim 7, "an enhanced joint test action group (EJTAG) compliant interface" is disclosed by Tabak page 466 FIG 21.7.
53. In claim 8, "a trace function" is disclosed by Tabak page 466 "trace".
54. MOTIVATION FOR CLAIMS 2-8. At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to use Tabak to modify Fletcher. One of ordinary skill in the art would have been motivated to do this in order to replace files that were accidentally lost or deleted.
55. Claims 9-14 are method claims with the same limitations are claims 1-8 above, and are rejected for the same reasons.
56. Claims 15-19 are "microprocessor, with an associated diagnostic module" claims with the same limitations as claim 1-8 above, and are rejected for the same reasons.

Additional Cited Prior Art

57. The following US patents or publications are hereby cited as prior art, but have not been used for rejection. Applicant should review these carefully before responding to this office action.
58. US Patent 5,291,586 by Jen, column 13 line 62 discloses "BACKUP register... state machine".
59. US Patent 6,107,852 by Durham, column 1 line 24 discloses "pipelines in microprocessors, general purpose state-machines".

Conclusion

60. All pending claims stand rejected.

Communication

61. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eduardo Garcia-Otero whose telephone number is 571-272-3711. The examiner can normally be reached on Monday through Thursday from 9:00 AM to 8:00 PM. If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Kevin Teska, can be reached at 571-272-3761. The fax phone number for this group is 703-872-9306.

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